

A M E N D M E N T

IN THE CLAIMS:

Please cancel claim 4 and amend claims 1, 5, 10, 17, and 20, so that the claims read as follows:

1. (Currently amended) A method of aligning signals from a first receiver located in a first clock domain to a second receiver located in a second clock domain, the method comprising the steps of:

creating a programmable delay element between the first and second receivers wherein creating the programmable delay element comprises:

providing at least one selectable delay for each of a first plurality of signal lines adapted to receive signals transmitted from the first receiver to the second receiver;
and

providing at least one selectable delay for each of a second plurality of signal lines adapted to receive signals transmitted from the second receiver to the first receiver;
and

selectively adding delay via the programmable delay element to the signals until the signals are aligned.

2. (Original) The method of claim 1 wherein creating the programmable delay element comprises providing at least one selectable delay for each of a plurality of signal lines between the first and second receivers.

3. (Original) The method of claim 2 wherein each selectable delay comprises a latch.

4. (Canceled)

5. (Currently amended) The method of claim ~~4~~ ⁴ wherein:
each selectable delay for the first plurality of signal lines comprises at least one latch that is clocked by a clock of the second clock domain; and

each selectable delay for the second plurality of signal lines comprises at least one latch that is clocked by a clock of the first clock domain.

6. (Original) The method of claim 1 wherein selectively adding delay via the programmable delay element to the signals until the signals are aligned comprises:

(a) testing operation of the first and second receivers in response to differing delays between signals transmitted between the first and second receivers;

(b) determining one or more delays that cause the first and second receivers to exchange signals without errors; and

(c) employing the one or more delays to align signals transmitted between the first and second receivers.

7. (Original) The method of claim ~~6~~ ⁶ wherein steps (a)-(c) are performed automatically.

8. (Original) A method of aligning signals transmitted between a first receiver located in a first clock domain and a

second receiver located in a second clock domain, the method comprising the steps of:

(a) providing at least one selectable delay for each of a first plurality of signal lines adapted to receive signals transmitted from the first receiver to the second receiver;

(b) providing at least one selectable delay for each of a second plurality of signal lines adapted to receive signals transmitted from the second receiver to the first receiver;

(c) testing operation of the first and second receivers in response to differing delays between signals transmitted between the first and second receivers;

(d) determining one or more delays that cause the first and second receivers to exchange signals without errors; and

(e) employing the one or more delays during subsequent transmission of signals between the first and second receivers.

8. (Original) The method of claim 8 wherein steps (c)-(e) are performed automatically.

9. (Currently amended) An apparatus for use with an asynchronous interface having first receiver that operates in a first clock domain, a second receiver that operates in a second clock domain, and a plurality of signal lines adapted to exchange signals between the first and second receivers, the apparatus comprising:

a first clock domain portion having at least a first delay circuit adapted to selectively introduce a first delay to a signal traveling from the second receiver to the first receiver via a first of the plurality of signal lines; and

a second clock domain portion having at least a second delay circuit adapted to selectively introduce a second delay to a signal traveling from the ~~second~~ first receiver to the ~~first~~ second receiver via a second of the plurality of signal lines.

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11. (Original) The apparatus of claim 10 wherein:

the first clock domain portion includes a first plurality of delay circuits, each of the first plurality of delay circuits adapted to selectively introduce a delay to a signal traveling from the second receiver to the first receiver via a different one of a first plurality of signal lines; and

the second clock domain portion includes a second plurality of delay circuits, each of the second plurality of delay circuits adapted to selectively introduce a delay to a signal traveling from the first receiver to the second receiver via a different one of a second plurality of signal lines.

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12. (Original) The apparatus of claim 11 wherein each delay circuit of the first plurality of delay circuits includes a plurality of selectable paths, each path having a different delay associated therewith.

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13. (Original) The apparatus of claim 12 wherein each path has a different number of latches associated therewith.

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14. (Original) The apparatus of claim 13 wherein at least one path has N-1 latches, wherein N equals the number of signal lines between the first and second receivers.

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15. (Original) The apparatus of claim 11 wherein each delay circuit of the second plurality of delay circuits includes a plurality of selectable paths, each path having a different delay associated therewith.

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16. (Original) The apparatus of claim 15 wherein each path has a different number of latches associated therewith.

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17. (Currently amended) An apparatus comprising:
an asynchronous interface having:

a first receiver that operates in a first clock domain;

a second receiver that operates in a second clock domain;

a plurality of signal lines adapted to exchange signals between the first and second receivers;

a supplemental asynchronous interface device (SAID) comprising:

a first clock domain portion having at least a first delay circuit adapted to selectively introduce a first delay to a signal traveling from the second receiver to the first receiver via a first of the plurality of signal lines; and

a second clock domain portion having at least a second delay circuit adapted to selectively introduce a second delay to a signal traveling from the ~~second~~ first receiver to the ~~first~~ second receiver via a second of the plurality of signal lines.

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18. (Original) The apparatus of claim 17 wherein the first receiver comprises a first state machine and the second receiver comprises a second state machine.

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19. (Original) The apparatus of claim 17 wherein:
the plurality of signal lines comprises:

a first plurality of signal lines that travel through the first portion of the SAID; and

a second plurality of signal lines that travel through the second portion of the SAID;

the first clock domain portion includes a first plurality of delay circuits, each of the first plurality of delay circuits adapted to selectively introduce a delay to a signal traveling from the second receiver to the first receiver via a different one of the first plurality of signal lines; and

the second clock domain portion includes a second plurality of delay circuits, each of the second plurality of delay circuits adapted to selectively introduce a delay to a signal traveling from the first receiver to the second receiver via a different one of the second plurality of signal lines.

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20. (Currently amended) A computer program product for aligning signals transmitted via an asynchronous interface between a first receiver located in a first clock domain and a second receiver located in a second clock domain, comprising: a medium readable by a computer, the computer readable medium having computer program code adapted to:

(a) test operation of the first and second receivers in response to differing delays between signals transmitted between the first and second receivers;

(b) determine one or more selectable delays that cause the first and second receivers to exchange signals without errors; and

(c) ~~causing~~ cause the asynchronous interface to employ the one or more selectable delays during subsequent transmission of signals between the first and second receivers wherein the asynchronous interface includes a plurality of signal lines.